REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application. In the present response, the Applicant has not amended, canceled, or added any claims. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-2 , 4-5, 8-9, 11-12, 15-16, and 18-19 under 35 U.S.C. §103

The Examiner has rejected Claims 1-2, 4-5, 8-9, 11-12, 15-16, and 18-19 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,381,721 to Warren in view of U.S. Patent No. 7,058,856 to Shinmori. The Applicant respectfully disagrees since the cited combination of Warren and Shinmori does not teach or suggest enabling a testing port based on a configuration of port inhibit circuitry as recited in independent Claims 1, 8, and 15.

The Examiner states that Warren discloses enabling a testing port based on a configuration of port inhibit circuitry. (*See* Examiner's Action electronically delivered March 2, 2007, pages 2, 3, and 4.) Warren teaches unidirectional data on a test data input signal TDI and a test output signal are encoded with start and stop bits. When a receive control signal recognizes two successive serial bits as being the start bits S1 and S2, the receive shift register 114 is controlled on the line 126 to serially load the next eight successive bits. The error detector 400 operates by detecting a lack of a stop bit in the incoming data stream. Once an error of this type has been detected, the error indicator is asserted which has the effect of inhibiting further data from being transmitted or received. (*See* column 9, lines 33-53.) Thus, Warren teaches that a lack of a stop bit in a data stream will inhibit data from being transmitted. As such, Warren does not teach enabling a testing port based on a configuration of port inhibit circuitry, but rather a on data stream passing through the test port.

Therefore, Warren does not teach enabling a testing port based on a configuration of port inhibit circuitry as recited in independent Claims 1, 8, and 15.

Furthermore, Warren does not suggest the same. Warren is directed to preventing communication between an integrated circuit and an interface to prevent garbage data being transmitted or received when power is disconnected from the integrated circuit while the interface (and off chip processing system) remain "powered up." Warren is further directed to prevent functional circuitry on the integrated circuit from attempting to transmit data off chip or attempting to analyze data received on-chip if a cable becomes physically disconnected from the connection port of the integrated circuit. (*See* column 1, lines 37-50.) In either case, Warren relies on real time information encoded in an existing test data input signal TDI data stream to enable a test port and, therefore, does not enable the test port independent of the test data input signal TDI. Since enabling a testing port in Warren is dependent on the test data input signal TDI, Warren does not enable a testing port based on a configuration of port inhibit circuitry. As such, Warren does not teach or suggest enabling a testing port based on a configuration of port inhibit circuitry and, therefore, does not establish a *prima facie* case of obviousness for independent Claims 1, 8, and 15 and Claims that depend thereon.

Shinmori has not been cited to cure this deficiency of Warren but to disclose modifiable inhibit circuitry to achieve a configuration that determines an extent to which a testing port is enabled. (*See* Examiner's Action electronically delivered March 2, 2007, pages 3 and 4.) Additionally, the Applicant does not find where Shinmori cures the above noted deficiency of Warren. As such, the cited combination of Warren and Shinmori does not establish a *prima facie* case of obviousness for independent Claims 1, 8, and 15 and Claims that depend thereon.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-2, 4-5, 8-9, 11-12, 15-16, and 18-19 and allow issuance thereof.

II. Rejection of Claims 3, 6-7, 10, 13-14, 17, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 3, 6-7, 10, 13-14, 17, and 20 under 35 U.S.C. §103(a) as being unpatentable over Warren in view of Shinmori and further in view of the following: U.S. Patent No. 7,124,340 to Bos, *et al.*, for dependent Claims 6 and 13; U.S. Patent No. 6,769,081 to Parulkar for dependent Claims 3, 10, and 17; and U.S. Patent No. 6,522,100 to Hansford for dependent Claims 7, 14, and 20. The Applicant respectfully disagrees.

As argued above, the cited combination of Warren and Shinmori does not establish a *prima facie* case of obviousness for independent Claims 1, 8, and 15 and Claims that depend thereon. The Applicant does not find where the above references cure the noted deficiency of Warren and Shinmori. Additionally, the above references have not been cited to cure this deficiency but to teach the subject matter of the above noted dependent claims. (*See* Examiner's Action electronically delivered March 2, 2007, pages 6 and 7.) Thus, the cited combinations do not establish a *prima facie* case of obviousness of independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 3, 6-7, 10, 13-14, 17, and 20 and allow issuance thereof.

III. Comment on References

The Applicant reserves further review of the references cited but not relied upon if relied upon in the future.

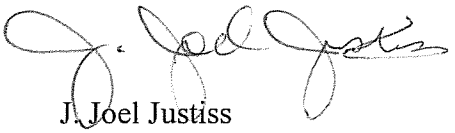
IV. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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Dated: June 4, 2007

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